

**WHAT IS CLAIMED IS:**

- 1        1. A method of forming an edge seal along a periphery of an integrated circuit  
2        device to provide increased corrosion and oxidation resistance to metallization of  
3        the integrated circuit device, the method comprising the steps of:
  - 4        a. providing a semiconductor substrate having a metallic feature therein;
  - 5        b. depositing a layer of dielectric material over the semiconductor substrate and  
6        metallic feature, the layer of dielectric material comprising a low-k dielectric material;
  - 7        c. selectively removing a portion of the layer of dielectric material to form a cavity  
8        and expose a portion of the metallic feature;
  - 9        d. conformally depositing a layer of an insulation material in the cavity and over the  
10       layer of dielectric material, wherein the insulation material and dielectric material are  
11       different materials;
  - 12       e. removing horizontal portions of the layer of insulation material so as to expose  
13       at least the metallic feature in the cavity;

- 14 f. depositing a barrier metal on the layer of insulation material in the cavity and on  
15 the exposed metallic feature;
- 16 g. depositing a high conductivity metal in the cavity to fill the cavity; and
- 17 h. planarizing the semiconductor substrate down to the layer of dielectric material.

1 2. The method of claim 1 wherein the low-k dielectric material comprises SiLK or  
2 fluoridized polyimide.

1 3. The method of claim 1 wherein the layer of dielectric material comprises a bottom  
2 layer on the semiconductor substrate, the low-k dielectric material on the bottom  
3 layer and a top moisture barrier on the low-k dielectric material.

1 4. The method of claim 1 wherein the insulation material is selected from the group  
2 consisting of  $\text{SiO}_2$ , SiC,  $\text{Si}_3\text{N}_4$ ,  $\text{Al}_2\text{O}_3$ , diamond like carbon, polyimide and  
3 combinations thereof.

1 5. The method of claim 1 wherein the barrier layer is selected from the group  
2 consisting of tantalum, tantalum nitride, chromium/ chromium oxide, titanium,  
3 titanium nitride, tungsten silicide and combinations thereof.

1 6. The method of claim 1 wherein the high conductivity metal is copper.

1 7. The method of claim 1 wherein the thickness of the insulation material in the  
2 cavity is 0.05 microns to 0.5 microns.

1 8. The method of claim 1 wherein the cavity comprises at least two contiguous  
2 cavities which form a damascene structure.

1 9. An edge seal around the periphery of an integrated circuit device comprising:

2 a. a semiconductor substrate;

3 b. a layer of dielectric material over the semiconductor substrate, the layer of  
4 dielectric material comprising a low-k dielectric material;

5 c. a metallic wall of a high conductivity metal in the layer of dielectric material; and  
6 d. a layer of insulation material between the metallic wall and the dielectric material,  
7 wherein the insulation material and dielectric material are different materials.

1 10. The edge seal of claim 9 wherein the low-k dielectric material comprises SiLK  
2 or fluoridized polyimide.

1 11. The edge seal of claim 9 wherein the layer of dielectric material comprises a  
2 bottom layer on the semiconductor substrate, the low-k dielectric material on the  
3 bottom layer and a top moisture barrier on the low-k dielectric material.

1 12. The edge seal of claim 9 wherein the insulation material is selected from the  
2 group consisting of  $\text{SiO}_2$ , SiC,  $\text{Si}_3\text{N}_4$ ,  $\text{Al}_2\text{O}_3$ , diamond like carbon, polyimide and  
3 combinations thereof.

1 13. The edge seal of claim 9 further comprising a barrier layer between the metallic  
2 wall and the insulation material wherein the barrier layer is selected from the group

3 consisting of tantalum, tantalum nitride, chromium/ chromium oxide, titanium,  
4 titanium nitride, tungsten silicide and combinations thereof.

1 14. The edge seal of claim 9 wherein the high conductivity metal is copper.

1 15. The edge seal of claim 9 wherein the thickness of the insulation material is 0.05  
2 microns to 0.5 microns.

1 16. The edge seal of claim 9 wherein there are two metallic walls in the at least one  
2 layer of dielectric material and there is a layer of insulation material between the  
3 dielectric material and each of the metallic walls with each layer of insulation  
4 material being of a different material than the dielectric material.

1 17. A method of forming an edge seal along a periphery of an integrated circuit  
2 device to provide increased corrosion and oxidation resistance to metallization of  
3 the integrated circuit device, the method comprising the steps of:

4 a. providing a semiconductor substrate having a metallic feature therein;

- 5 b. depositing a layer of dielectric material over the semiconductor substrate and  
6 metallic feature, the layer of dielectric material comprising a low-k dielectric material;
- 7 c. selectively removing a portion of the layer of dielectric material to form two first  
8 cavities and expose a portion of the metallic feature;
- 9 d. depositing an insulation material to fill the two first cavities, wherein the insulation  
10 material and dielectric material are different materials;
- 11 e. selectively removing a portion of the layer of dielectric material, and any overlying  
12 insulation material to form a second cavity;
- 13 f. depositing a barrier metal in the second cavity and on the exposed metallic  
14 feature;
- 15 g. depositing a high conductivity metal in the second cavity to fill the cavity; and
- 16 h. planarizing the semiconductor substrate down to the layer of dielectric material.

1 18. An edge seal around the periphery of an integrated circuit device comprising:

- 2       a. a semiconductor substrate;
- 3       b. a layer of dielectric material over the semiconductor substrate, the layer of
- 4       dielectric material comprising a low-k dielectric material;
- 5       c. a metallic wall in the layer of dielectric material; and
- 6       d. a wall of insulation material between the metallic wall and the periphery of the
- 7       integrated circuit device wherein the insulation material and dielectric material are
- 8       different materials.